International Journal of Engineering Science Invention
ISSN (Online): 2319 – 6734, ISSN (Print): 2319 – 6726
www.ijesi.org Volume 2 Issue 10 ǁ October. 2013 ǁ PP.20-23

A New Approach to the Design and Implementation of Multipliers Using Reversible Logic

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ABSTRACT: *Reversible logic is gaining interest in the recent past years due to its less heat dissipating characteristics. It has been proved that any Boolean function can be implemented using reversible gates. Reversible logic gates are very much in demand for the future computing technologies as they are known to produce zero power dissipation under ideal conditions. Reversible logic circuits are of interests to power minimization having applications in low power CMOS design, optical information processing DNA computing, bioinformatics, quantum computing and nanotechnology. Reversible logic synthesis circuits are very important issues in this area. Multipliers are very essential for the construction of various computational units of a quantum computer. Multiplier is an important hardware unit that decides the speed in any processor. In this work, an unsigned four bit array multiplier using reversible gates are implemented.*

KEYWORDS: *Multipliers, New RSgate, Reversible logic, Quantum cost.*

I. INTROUCTION

Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. According to Landauer's research, the amount of energy dissipated for every irreversible bit operation is at least KTln2 joules, where K=1.3806505*10-23m2kg-2K-1 (joule/Kelvin-1) is the Boltzmann's constant and T is the temperature at which operation is performed [1]. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components In 1973, Bennett showed that KTln2 energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs. Reversible logic marks a promising new direction where all operations are performed in the domain of low-power design since reversible circuits might have zero power dissipation [2, 3]. Computing systems give off heat when voltage levels change from positive to negative: bits from zero to one. Most of the energy needed to make that change is given off in the form of heat. Rather than changing voltages to new levels, reversible circuit elements will gradually move charge from one node to the next. This way, one can only expect to lose a minute amount of energy on each transition. Reversible computing strongly affects digital logic designs. Reversible logic elements are needed to recover the state of inputs from the outputs. In [4], first reversible circuits driven by their input signals only (and accordingly without additional power supplies) already have been implemented. Besides that also, the growing area of quantum computation [5] established itself as a promising application of reversible logic. To realize a reversible logic circuit some restrictions must be considered, i.e. fan outs and feedback are not allowed [5]. In this paper, one of the important building blocks in most of the computing systems, multiplier is designed using reversible logic gates in the direction to optimize the quantum parameters which decide the performance of a reversible logic circuit. Reversible multipliers may be optimized by introducing new gates.Rest of the paper is organized as follows: SectionII gives basic reversible logic circuits section III gives the reversible multiplier and novel design of reversible unsigned and signed multipliers and finally section IV concludes the paper.

II. REVERSIBLE LOGIC CIRCUITS

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits. The number of Reversible gates (N): The number of reversible gates used in circuit. The number of constant inputs (CI) refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function. The number of garbage outputs refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve

reversibility. Quantum cost (QC) refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.

1.1 Basic reversible logic circuits

1.1.1: Feynman Gate/CNOT Gate: Fig.1 shows a 2*2 Feynman gate. The input vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by P=A, Q=A⊕B. Quantum cost of a Feynman gate is 1.

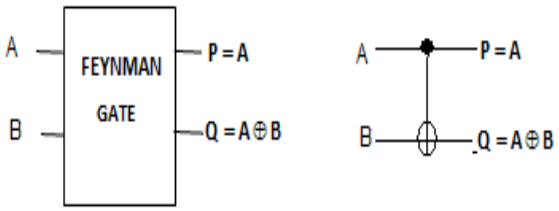

Figure 1: Feynman gate

1.1.2: Toffoli Gate: Fig.2 shows a 3*3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5.

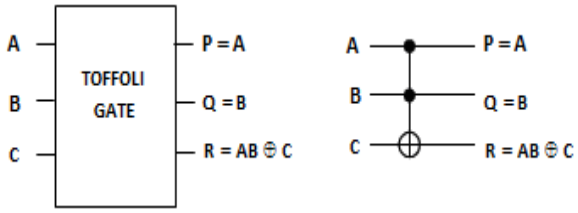

Figure 2: Toffoli gate

1.1.3: Peres Gate: Fig .3 shows a 3*3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A⊕B and R=AB⊕C. Quantum cost of a Peres gate is 4.

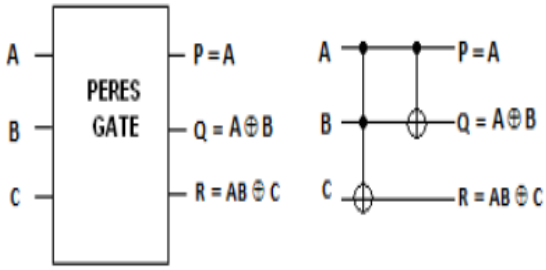

Figure 3: Peres gate

1.1.4: Double Peres gate (DPG): Fig .4 shows a Double Peres Gate. The full adder using DPG is obtained with C=0 and D= Cin and its quantum cost is 6.

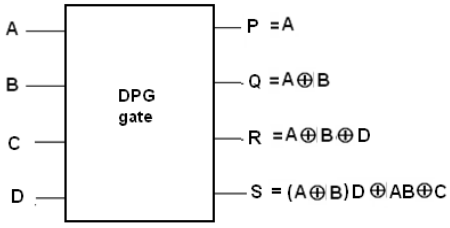

Figure 4: Double peres gate

III. REVERSIBLE MULTIPLIERS

Multiplier circuits are of special importance because of the fact that they are the integral component of every computer system, cellular phone etc. Multiplier circuits play an important role in reversible computation, which is helpful in diverse areas such as low power CMOS design. It is important for every processor to have low power and a high speed multiplier.

In addition to the available basic reversible gates, new gates are invented in order to optimize reversible circuits in terms of quantum parameters. The new RS gate is proposed to implement reversible multipliers. This new RS gate is implemented using 2 CNOT gates function as a xor gate and AND operation is implemented using FRG gate and the quantum cost of RSG gate is 10.The new RS gate reduces the gate count when compared to the earlier RS gate which was implemented using CNOT gates and the two Peres gates. The new RS gate is shown inFig.5 along with its quantum representation.

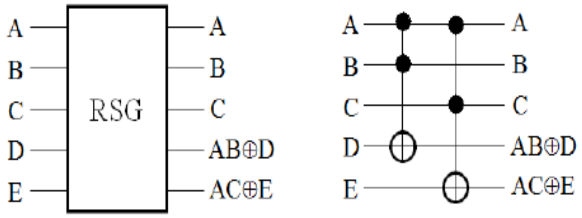

Figure 5: New RS gate and its Quantum representation

1.1 Reversible signed multiplier: Design of multiplier using reversible logic gates is done by Partial product generation(PPG) and Multi-operand addition(MOA).

1.1.1 Partial Product Generation: The circuit for partial product generation is same for both unsigned and signed multipliers. In the previous multiplier designs partial products are generated using Peres gates, and in order to apply these product terms to multi - operand addition circuit, copying gates are required because of fanout restriction in reversible logic circuits. In this paper, the use of proposed RS gate not only reduces the number of gates required to produce product terms but also provide the required number of product terms that avoids the necessity of copying gates. The PPG circuit is shown in fig 6.

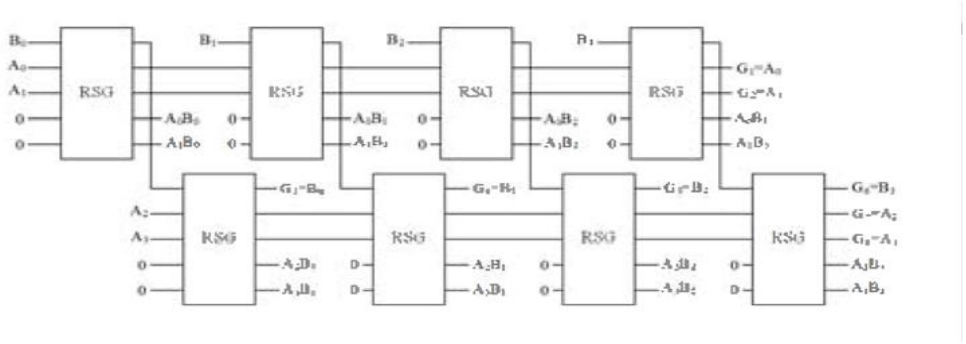

Figure 6: Partial Product Generation

1.1.2 Multi – Operand addition: The product terms generated from the PPG circuit are to be added to achieve the multiplier operation. DPG and Peres gates will function as full adder and half adder respectively for MOA. Fig. 7 shows the MOA for unsigned binary multiplier.

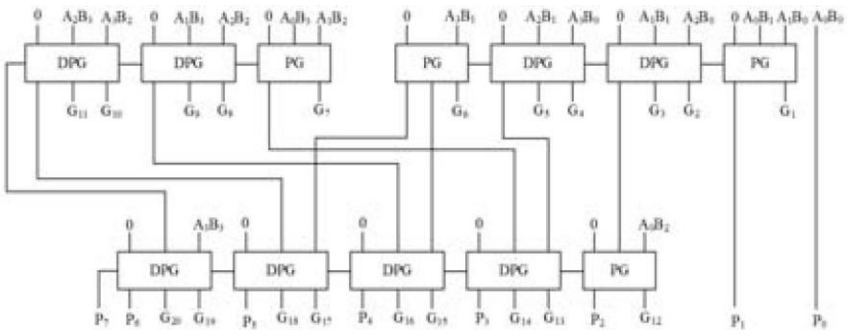

Figure 7: MOA of Reversible unsigned multiplier

1.2: Reversible Signed Multiplier: Signed multiplication is having great importance in digital circuits. In this paper, a reversible signed multiplier is proposed based on conventional Baugh-Wooley multiplier that works on two's complement of the operands. For signed multiplication, the same product terms that are generated from

fig.6 can be used but the application of those terms to the MOA circuit requires additionally six NOT gates as shown in fig. 8.

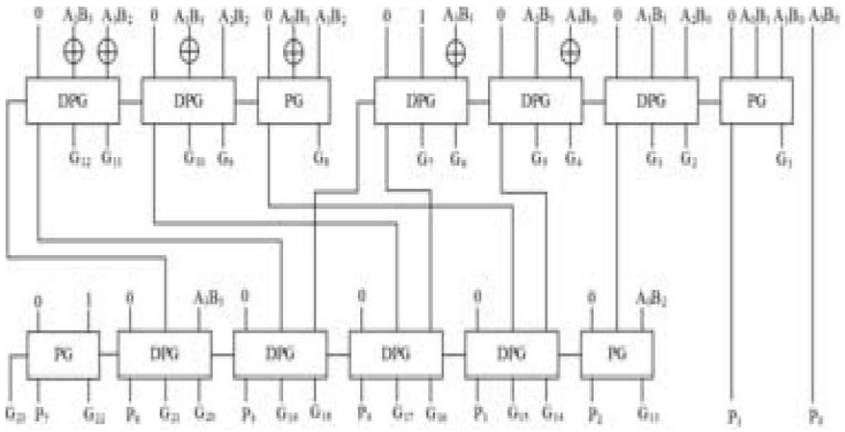

Figure 8: MOA of reversible signed multiplier

IV. IMPLEMENTATION RESULTS

The number of gates required for PPG and MOA are 8 and 12 respectively giving a total of 20. The garbage outputs are 28 (PPG - 8 and MOA - 20), among which 8 are reproduction of inputs. Quantum cost of the circuit is 137. The proposed signed multiplier is designed using a total of 27 gates (NOT - 6, RSG - 8, PG - 4, D PG - 9) with 29 inputs as constant, producing 31 garbage outputs and its quantum cost is 150.Reversible unsigned and signed multiplier circuits are implemented on Xilinx platform from which delay and power values obtained and are given in table1.

Reversible Multiplier	Power (mW)	Delay (nS)
Unsigned	28.7	16.322
Signed	28.65	16.646

Table 1: Implementation results of reversible multipliers.

V. CONCLUSION

Lot of scope is there to optimize the reversible circuits by inventing new gates. The proposed new RS gate reduces the gate count by 35%. Reversible unsigned multiplier is optimized in terms of gate count as the remaining quantum parameters are upto the optimization mark. Reversible signed multiplier based on Baugh - Wooley multiplier is also proposed in this paper.

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